CLAIMS

What is claimed is:

1. A digital signal processing system that comprises:

a plurality of processor subsystems that each include:

a processor core; and

a direct memory access ("DMA") controller;

a external input/output port ("XPORT") coupled to each of the processor cores and each of the DMA controllers via a multiplexer; and

an XPORT arbiter coupled to the multiplexer and configured to grant XPORT access to a selected one of the processor cores and DMA controllers.

2. The system of claim 1, wherein the multiplexer, XPORT arbiter, and the plurality of processor subsystems are fabricated on a single chip.

3. The system of claim 1, wherein the XPORT arbiter is configured to provide a HOLD signal to the processor cores, wherein the HOLD signal is asserted in response to the assertion of one or more request signals from the DMA controllers.

4. The system of claim 3, wherein the XPORT arbiter includes a logic gate configured to assert the HOLD signal in response to the assertion of any one of a plurality of request signals, wherein the DMA controllers assert a corresponding one of said request signals to request access to the XPORT.

5. The system of claim 3, wherein the processor cores are each configured to assert a respective HOLD acknowledge signal in response to an assertion of the HOLD signal if the processor core is currently not accessing the XPORT.

6. The system of claim 5, wherein the XPORT arbiter includes a logic gate configured to combine the HOLD acknowledge signals to produce a combined acknowledge signal, wherein the logic gate asserts the combined acknowledge signal only when each of the HOLD acknowledge signals is asserted.

7. The system of claim 6, wherein the XPORT arbiter further includes a DMA arbiter configured to receive the request signals from the DMA controllers and further configured to assert a conditional grant signal for a selected DMA controller in response to the assertion of a request signal.

8. The system of claim 7, wherein the XPORT arbiter further includes a grant signal gate for each DMA controller, wherein each grant signal gate is configured to assert a grant signal to a selected DMA controller when both the combined acknowledge signal and the conditional grant signal for the selected DMA controller are asserted.

9. The system of claim 7, wherein the XPORT arbiter further includes a processor core arbiter distinct from the DMA arbiter.

10. The system of claim 9, wherein the processor subsystems each further include a register coupled between the processor core and the processor core arbiter, wherein the register includes a request bit and a grant bit.

11. The system of claim 10, wherein the processor cores execute software including an XPORT arbitration process, wherein the process asserts the request bit to request access to the XPORT, and wherein the process accesses the XPORT only if the grant bit is asserted subsequent to the assertion of the request bit.

12. The system of claim 11, wherein the processor core arbiter asserts a grant bit for a selected processor core in response to the assertion of one or more request bits.

13. A method of providing access to a limited resource in a digital signal processing system, wherein the method comprises:

receiving one or more request signals from a set of components of two distinct types;

responsively asserting a grant signal to a selected component of a first type if the one or more request signals are each from components of the first type; and

responsively asserting a hold signal to each component of the first type if the one or more request signals include a request signal from a component of the second type.

14. The method of claim 13, further comprising:

if the one or more request signals include a request signal from a component of the second type:

receiving assertions of hold acknowledge signals from each of the components of the first type;

asserting a grant signal to a selected component of the second type after receiving said hold acknowledge signal assertions.

15. The method of claim 14, wherein the components of the first type assert each assert a respective hold acknowledge signal in response to assertion of the hold signal, and wherein any component of the first type that is actively accessing the XPORT delays assertion of the hold acknowledge signal until said accessing is completed.

16. The method of claim 15, wherein after asserting their hold acknowledge signals, the components of the first type stall any of their accesses until after the hold signal is de-asserted.

17. The method of claim 13, wherein after asserting the request signal, the components of the first type monitor the grant signal for assertion, wherein the components of the first type access the limited resource after detecting said grant signal assertion, and wherein the components of the first type de-assert the request signal after completing said access.

18. The method of claim 13, wherein the components of the first type are processor cores.

19. The method of claim 13, wherein the components of the second type are DMA controllers.

20. The method of claim 13, wherein the limited resource is an external input/output port that can be used by only one of said components at a time.